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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10067151	01/29/2002	716	16	2825	DO

**APPLICANTS: Rupp Charles; Garverick Timothy; Arnold Jeffrey;

**CONTINUING DATA VERIFIED:

THIS APPLN CLAIMS BENEFIT OF 60/265,303 01/30/2001

YES TD

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		ATTORNEY DOCKET NO	
35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		STRE-003/01US	
Verified and Acknowledged Examiners's initials TD			
TITLE : Design methodology for merging programmable logic into a custom IC			
U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)			

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	Total Claims
			Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drawn	Figs. Drawn
			Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner	Application Examiner
		PREPARED FOR ISSUE	
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